Programmes After Market Services
NPB-1NB Series Transceivers

System Module

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Functional Description

NPB-1NB basic transceiver consists of a System/RF module (GB9), SW module and assembly parts. The keyboard matrix is located in the System/RF module. Display module, speaker, vibrator, handsfree/headset connector including microphone, SIM connector and buzzer are connected to the PCB via springs.

The system blocks provide the MCU, DSP and logic control functions in MAD2WD1 ASIC, external flash and RAM memories, audio processing and RF control hardware in COBBA GJP ASIC. Power supply circuitry CCONT supplies the operating voltages for the baseband and the RF blocks. CHAPS controls the input voltage and charging. The purpose of the RF block is to receive and demodulate the radio frequency signal from the base station and to transmit a modulated RF signal to the base station.

Modes of Operation

The transceiver has five different operation modes:

- Power off mode
- Idle mode
- Active mode
- Charge mode
- Local mode

In the **power off mode** only the circuits needed for power up are supplied.

In the **idle mode** circuits are powered down and only sleep clock is running.

In the **active mode** all the circuits are supplied with power although some parts might be in the idle state part of the time.

The **charge mod**e is effective in parallel with all previous modes. The charge mode itself consists of two different states, i.e. the fast charge and the maintenance mode.

The **local mode** is used for alignment and testing.

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Baseband Module

Technical Summary

The system (baseband) module includes four ASICs: CHAPS, CCONT, COBBA-GJP and MAD2WD1, which take care of the baseband functions of the engine. The baseband is designed to work with a DCT-4 type direct conversion RF.

The baseband is running from a 2.8V power rail, which is supplied by a power controlling ASIC CCONT. In the CCONT there are 6 individually controlled regulator outputs for RF-section and two outputs for the baseband. In addition there is one +5V power supply output (V5V). The CCONT contains also a SIM interface, which supports both 3V and 5V SIM-cards. A real time clock function is integrated into the CCONT, which utilizes the same 32kHz clock supply as the sleep clock. The MAD is a dual voltage circuit using VBB (2.8V Baseband supply) and VCORE (1.8V. Core Voltage supply for MAD2WD1 ver. C05).

The interface between the baseband and the RF section is mainly handled by a COBBA ASIC. COBBA provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths and also A/D and D/A conversions of received and transmitted audio signals to and from the user interface. The COBBA supplies the analog TXC and AFC signals to RF section according to the MAD DSP digital control. Data transmission between the COBBA and the MAD is implemented using serial bus for high speed signaling and for PCM coded audio signals. Digital speech processing is handled by the MAD ASIC. COBBA is a dual voltage circuit, the digital parts are running from the baseband supply VBB and the analog parts are running from the analog supply VCOBBA.

The baseband supports both internal and external microphone inputs and speaker outputs. Input and output signal source selection and gain control is done by the COBBA according to control messages from the MAD. Keypad tones, DTMF, and other audio tones are generated and encoded by the MAD and transmitted to the COBBA for decoding.

An UI-Switch N400 is used as HW-driver for: LEDs, Buzzer and Vibra. Buzzer and Vibra (internal) alert control signals are generated by the MAD with separate PWM outputs.

The baseband architecture supports a power saving function called "sleep mode". This sleep mode shuts off the VCTCXO, which is used as system clock source for both RF and baseband. During the sleep mode the system runs from a 32 kHz crystal. The phone is waken up by a timer running from this 32 kHz clock supply. The sleeping time is determined by some network parameters. The sleep mode is entered when both the MCU and the DSP are in standby mode and the normal VCTCXO clock has been switched off.

The battery charging is controlled by a PWM signal from the CCONT. The PWM duty cycle is determined by a charging software and is fed to the CHAPS charging switch.

The NPB-1NB transceiver supports 'ELVI' (DCT3) and 'Janette' (DCT4) chargers, both 2-wire and 3-wire, but when using 3-wire chargers, then the 3. wire (charger control input) is connected to Ground by the phone.

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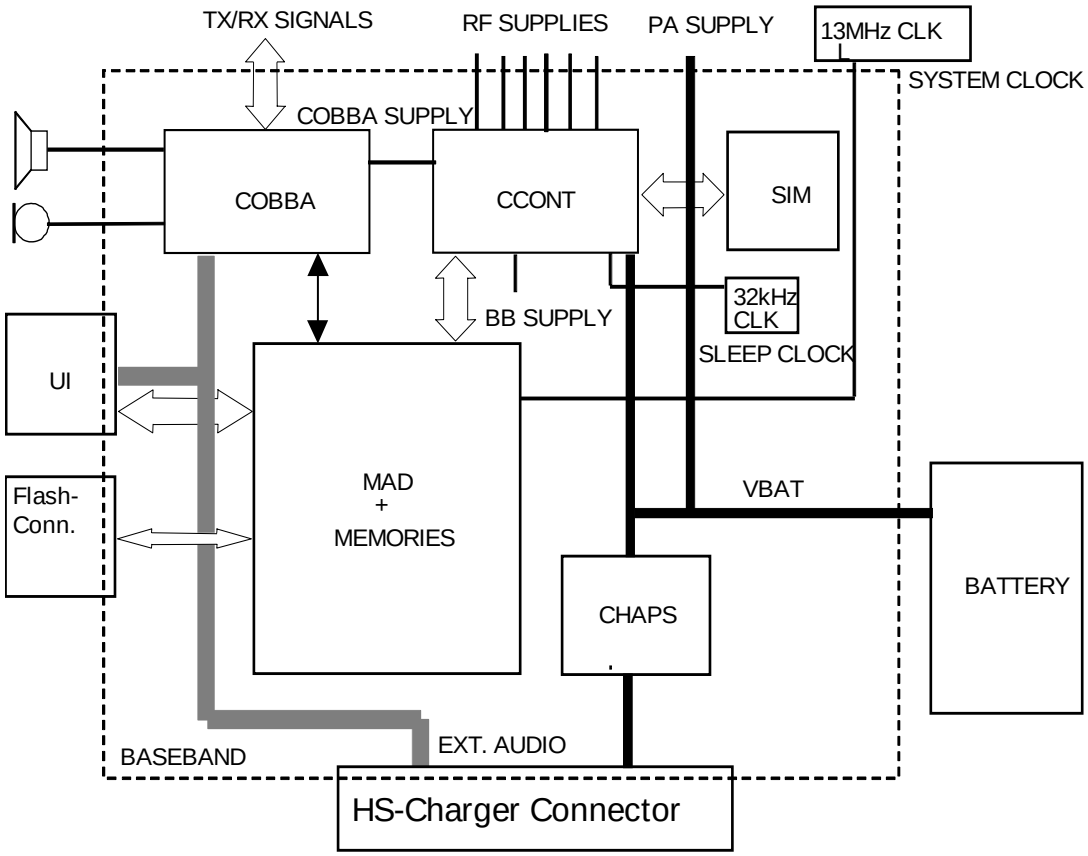

Figure 1: Baseband Block Diagram

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Technical Specifications

Table 1: Absolute maximum ratings

Parameter	Rating
Battery voltage	-0.3 ... 5.3 V
Charger input voltage	-5.0 ... 30V (Varistor Clamp voltage)

DC Characteristics

Table 2: Supply voltages, power consumption

Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply battery voltage	3.1	3.9	5.3	V
Battery power-up voltage (HW)	2.9	3.0	3.1	V
Battery cut off voltage (HW)	2.6	2.8	2.9	V (3.1 V SW cutoff)
Regulated baseband supply (VBB) voltage	2.7	2.8	2.85	V
Regulated baseband supply (VBB) current	3	50	125	mA
COBBA analog supply (VR6) voltage	2.7	2.8	2.85	V
COBBA analog supply (VR6) current	0	-	80	mA
Regulated 5V supply voltage	4.8	5.0	5.2	V
Regulated 5V supply current	0	-	30	mA
Regulated 5V SIM supply voltage	4.8	5.0	5.2	V
Regulated 5V SIM supply current	0	-	30	mA
Regulated 3V SIM supply voltage	2.8	3.0	3.2	V
Regulated 3V SIM supply current	0	-	30	mA
Voltage reference	1.4775	1.5	1.5225	V

External Signals and Connections

Battery Connector

The electrical specifications for the battery connector is shown in Table 3. The BSI contact on the battery connector is used to detect when the battery is to be removed to be able to shut down the operations of the SIM card before the power is lost if the battery is removed with power on.
The BSI contact disconnects earlier than the supply power contacts to give enough time for the SIM shut down.

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Table 3: Battery Connector

Pin/Conn	Line Symbol	Minimum	Typical /Nom	Maximum	Unit / Notes
1 / X803	VBATT	3.0	3.9	4.2	V / Battery voltage
2 / X803	BSI	0		2.85	V / Battery size indication Phone has 100kohm pull up resistor. SIM Card removal detection (Threshold is 2.4V@VBB=2.8V)
3 / X803	BTEMP	0		1.4	V / Battery temperature indication Phone has a 150k (+-5%) pullup resistor, Battery package has a NTC pulldown resistor: 47kW +-5%@+25C , B=4050+-3%
		2.1 5	 10	3 20	V / Phone power up by battery (input) ms / Power up pulse width
		1.9 90	 100	2.85 200	V / Battery power up by phone (output) ms / Power up pulse width
		0		1	kohm / Local mode initialization (in production)
4 / X803	BGND	0		0	V

DC (Charger) Connector

DC (charger) connector is physically integrated in the same component with the accessory interface connector. DC connector has both jack and contact pads for desk stand. An internal 1.5A Fuse in serial with Vin protects the phone against hazardous temperature rises caused by serious Charge-failures including over-voltage.

Table 4: System Connector - Charger Connection

Pin/Conn	Line Symbol	Minimum	Typical /Nom	Maximum	Unit / Notes
3 / X200	CHRGR+	0 0	8.4	12 850	V MA
4 / X200	CHRGR-	0	0	0.3	V

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Service (Flash/Test) Connector

The Test Flash-Connector is used as a flash programming interface for updating (i.e. re-programming) the flash program memory and as an electrical interface for access to the engine by service-tool (e.g. WinTesla). This Interface is typically used by Aftersales via a 'Hda52 Service battery' . The Connector is made as 4 Test Pads which are accessible through the mechanic of the phone when the Battery is removed.

When the flash programming-tool is connected to the phone (via 'Service battery'), supply power is provided through the battery contacts and the phone is powered up with a pulse given to the BTEMP line**.**

ESD protection is applied to all pads of X201.

Table 5: System Connector - Charger Connection

Pin/Conn	Line Symbol	Minimum	Typical /Nom	Maximum	Unit / Notes
3 / X200	CHRGR+	0 0	8.4	12 850	V MA
4 / X200	CHRGR-	0	0	0.3	V

SIM Card Connector

The SIM I/F does not support any other voltages than 3V and 5V.
The SIM card connector is located on the engine board beside the battery pack.

Table 6: SIM Card Connector

Pin/Conn	Line Symbol	Minimum	Typical /Nom	Maximum	Unit / Notes
1 / X400	SIMCLK		3.25 25		MHz / Frequency ns / T_{rise}/T_{fall}
2 / X400	SIMRST	4.0 2.8	"1" "1"	VSIM VSIM	V / 5V SIM card V / 3V SIM card
3,5 / X400	VSIM	4.8 2.8	5.0 3.0	5.2 3.2	V / 5V SIM card V / 3V SIM card
4 / X400	GND	0		0	V
6 / X400	DATA	4.0 0 2.8 0	"1" "0" "1" "0"	VSIM 0.5 VSIM 0.5 1	V / 5V Vin/Vout V / 3V Vin/Vout us / T_{rise}/T_{fall}

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Power Distribution

In normal operation the baseband is powered from the phone's battery. The baseband contains the parts that control power distribution to the whole phone excluding those components that use continuous battery supply. The battery feeds power directly to the CCONT and UI (buzzer and display/ keyboard lights).

An external charger can be used for recharging the battery and supplying power to the phone. The power management circuit CHAPS provides protection against over-voltages, charger failures and pirate chargers etc. that would otherwise cause damage to the phone.

Baseband power distribution is illustrated in the figure below.

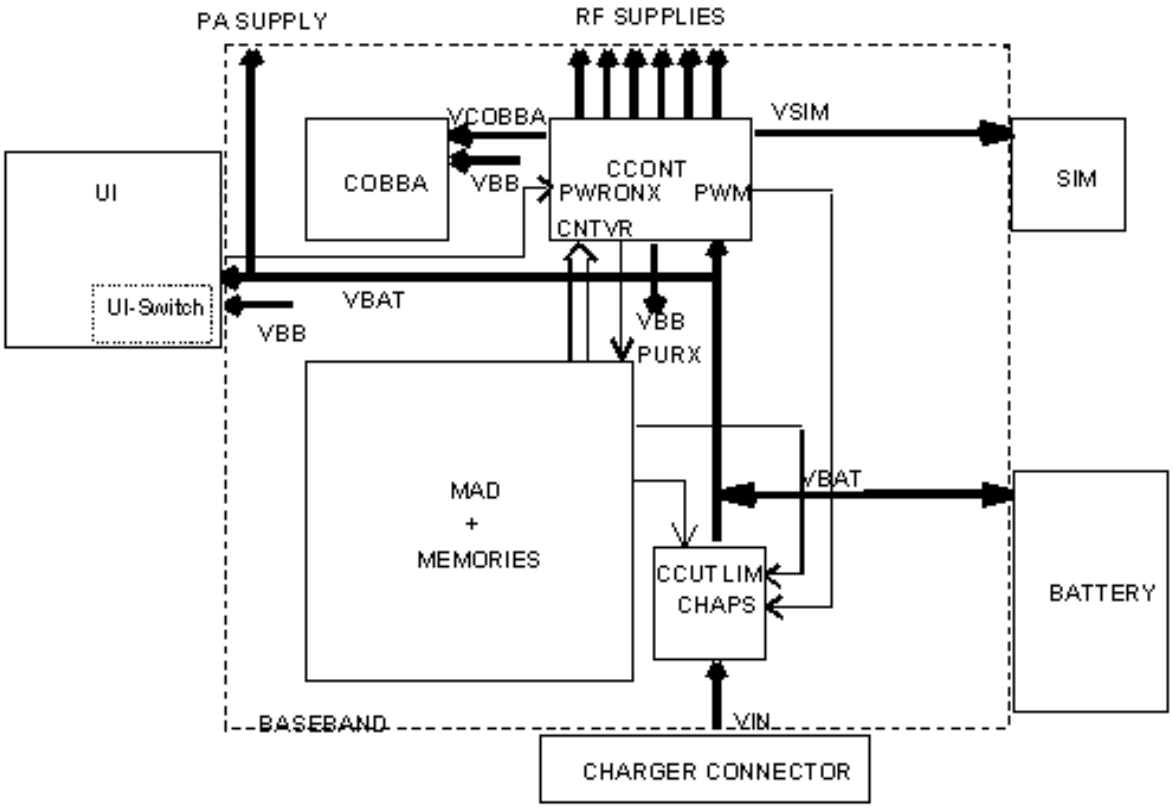

Figure 2: Power Distribution - Baseband

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RF regulators of the CCONT are connected to HAGAR and controlled directly using SYNPWR. Different modes are switched on via serial bus. Use of the regulators can be seen in the RF power distribution diagram.

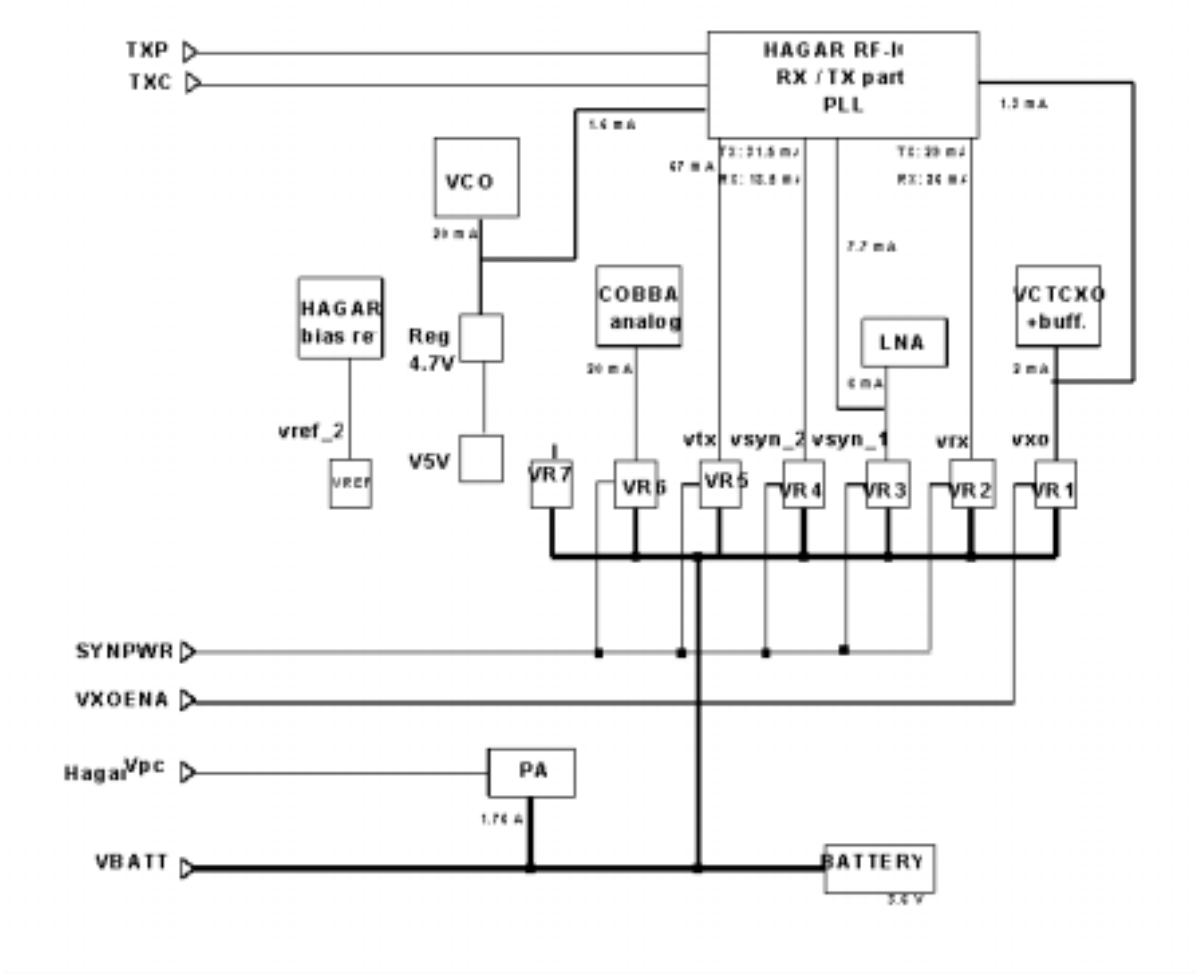

Figure 3: Power Distribution - RF

All control signals are coming from MAD2 (2.8 V logic signals).

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Table 7: RF Voltage Supplies

Volt. Source	Name of the supply	Load
V5V	VCP	PLL charge pump, VCO
VR5	VTX	TX modulator
VR1	VXO	VCTCXO
VR2	VRX	HAGAR IC (LNA+mixer+DTOS)
VR4	VSYN_2	HAGAR IC (div+LO- buff+prescaler)
VR3	VSYN_1	LNA + HAGAR (Vdd_bb)
VR6		COBBA analog parts
VREF_2		Ref. Voltage for HAGAR
RXREF (COBBA)		Ref. Voltage for HAGAR
TXVDCS (Hagar)		Ant. Sw. DCS
TXVDET (Hagar)		Power detector
Vbatt	VBATT	RF regulators in CCONT, PA

Battery Charging

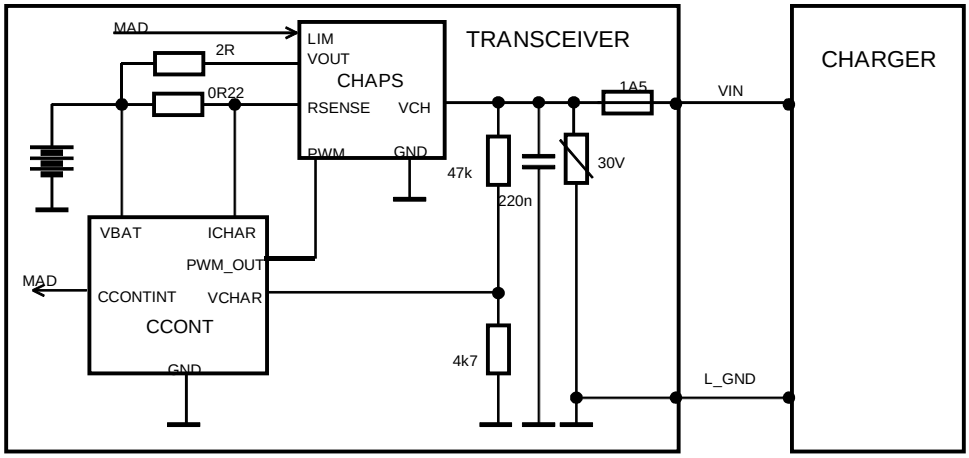

Figure 4: Charging block diagram

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Startup Charging

When a charger is connected, the CHAPS is supplying a startup current minimum of 130mA to the phone. The startup current provides initial charging to a phone with an empty battery. Startup circuit charges the battery until the battery voltage level reaches 3.0V (+/- 0.1V) and the CCONT releases the PURX reset signal and program execution starts. Charging mode is changed from startup charging to PWM charging that is controlled by the MCU software. If the battery voltage reaches 3.55V (3.75V maximum) before the program has taken control over the charging, the startup current is switched off. The startup current is switched on again when the battery voltage is sunken 100mV (nominal).

Table 8: Startup characteristics

Parameter	Symbol	Min	Typ	Max	Unit
VOUT Start- up mode cutoff limit	Vstart	3.45	3.55	3.75	V
VOUT Start- up mode hysteresis NOTE: Cout = 4.7 uF	Vstarthys	80	100	200	mV
Start-up regulator output current VOUT = 0V ... Vstart	Istart	130	165	200	mA

Battery Over-Voltage Protection

Output over-voltage protection is used to protect phone from damage. This function is also used to define the protection cutoff voltage for different battery types (Li or Ni). The power switch is immediately turned OFF if the voltage in VOUT rises above the selected limit VLIM.

Table 9: VLIM characteristics

Parameter	Symbol	LIM input	Min	Typ	Max	Unit
Output voltage cutoff limit (during transmission or Li-battery)	VLIM	LOW	4.4	4.6	4.8	V

The voltage limit (VLIM1 or VLIM2) is selected by logic LOW or logic HIGH on the CHAPS (N200) VLIM input pin.

When the switch in output over-voltage situation has once turned OFF, it stays OFF until the battery voltage falls below VLIM and PWM = LOW is detected. The switch can be turned on again by setting PWM = HIGH.

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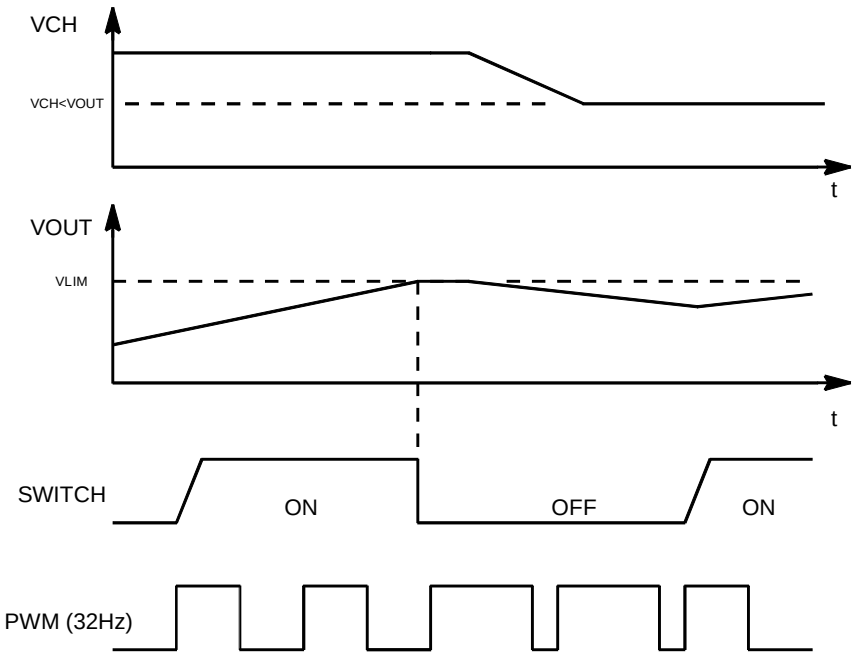

Figure 5: Output overvoltage protection

Battery Removal During Charging

Output over-voltage protection is also needed in case the main battery is removed when charger connected or charger is connected before the battery is connected to the phone.

With a charger connected, if VOUT exceeds VLIM, CHAPS turns switch OFF until the charger input has sunken below Vpor (nominal 3.0V, maximum 3.4V). MCU software will stop the charging (turn off PWM) when it detects that battery has been removed. The CHAPS remains in protection state as long as PWM stays HIGH after the output over-voltage situation has occurred.

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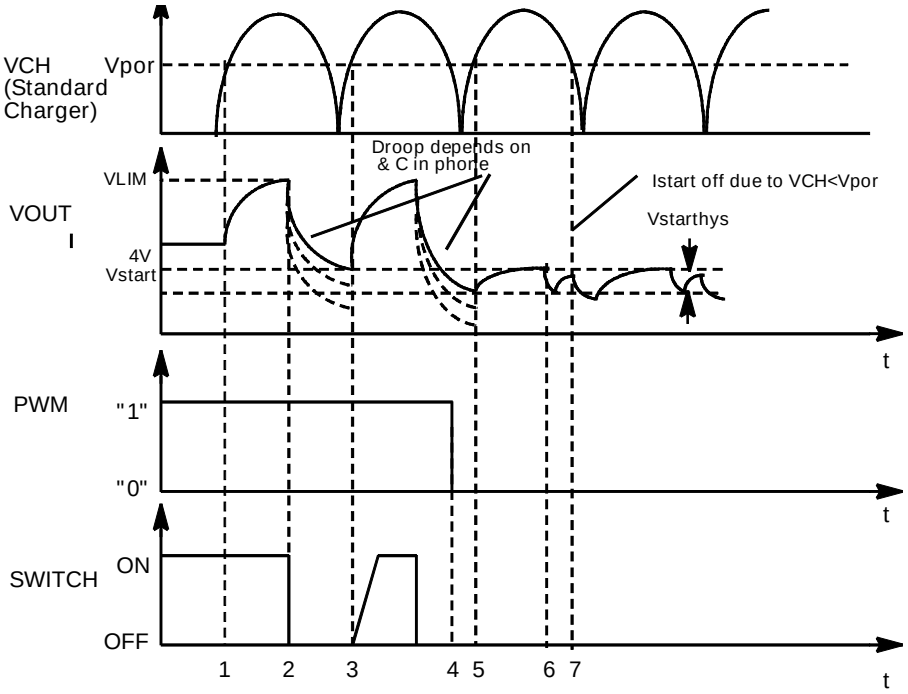

1. Battery removed, (standard) charger connected, VOUT rises (follows charger
2. VOUT exceeds limit VLIM(X), switch is turned immediately
3. VOUT falls (because no battery) , also VCH<Vpor (standard chargers full-output). When VCH > Vpor and VOUT < VLIM(X) -> switch turned on again (also is still HIGH) and VOUT again exceeds
4. Software sets PWM = LOW -> CHAPS does not enter PWM
5. PWM low -> Startup mode, startup current flows until Vstart limit
6. VOUT exceeds limit Vstart, Istart is
7. VCH falls below

Figure 6: Output overvoltage protection -battery removed

PWM

When a charger is used, the power switch is turned ON and OFF by the PWM input. PWM rate is 1Hz. When PWM is HIGH, the switch is ON and the output current Iout = charger current - CHAPS supply current. When PWM is LOW, the switch is OFF and the output current Iout = 0. To prevent the switching transients inducing noise in audio circuitry of the phone soft switching is used.

Battery Identification

Different battery types are identified by a pull-down resistor inside the battery pack. The BSI line inside transceiver has a 150k pull-up to VBB. The MCU can identify the battery by reading the BSI line DC-voltage level with a CCONT (N201) A/D-converter.

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Table 10: Battery identification

Name	Min	Typ	Max	Unit	Notes
BSI	0		2.8	V	Battery size indication 150k pullup resistor to VBB in phone SIM Card removal detection (Treshold is 2.4V@VBB=2.8V)
	-1%	5,6	+1%	kohm	Indication of a BMC-3 battery
	20	22	24	kohm	Indication resistor for a service battery
	-5		5	%	Indication resistor and pull-up resistor tolerance

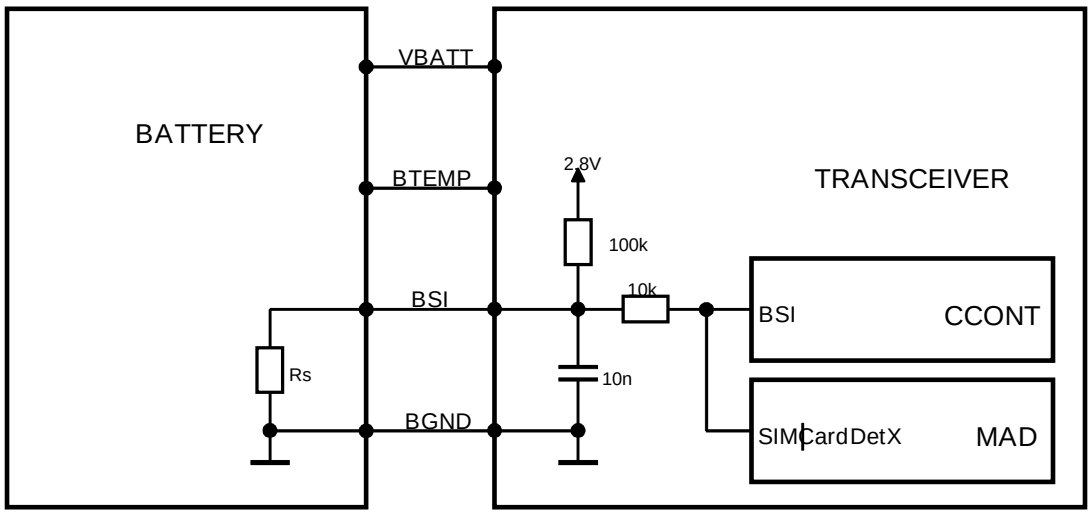

Figure 7: BSI connection- all batteries

The battery identification line is used also for battery removal detection. The BSI line is connected to a SIMCardDetX line of MAD2. SIMCardDetX is a threshold detector with a nominal input switching level 0.85xVcc for a rising edge and 0.55xVcc for a falling edge. The battery removal detection is used as a trigger to power down the SIM card before the power is lost. The BSI contact in the battery contact disconnects before the other contacts so that there is a delay between battery removal detection and supply power off.

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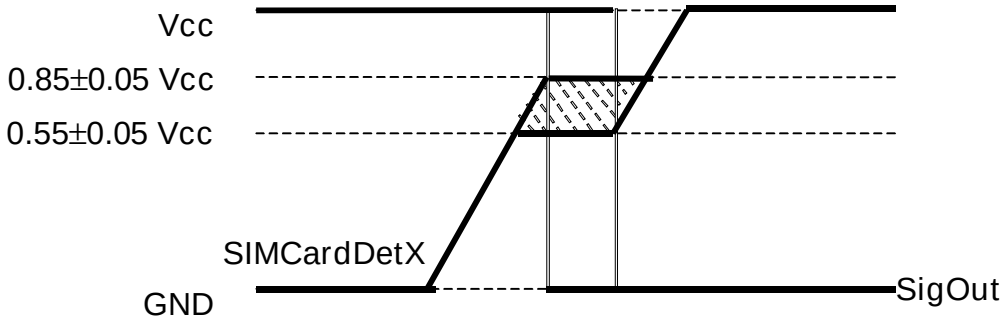

Figure 8: SIMCardDetX detection levels

Battery Temperature

The battery temperature is measured with a NTC inside the battery pack. The BTEMP line inside transceiver has a 100k pull-up to VREF. The MCU can calculate the battery temperature by reading the BTEMP line DC-voltage level with a CCONT (N201) A/D-converter.

Table 11: Battery temperature

Name	Min	Typ	Max	Unit	Notes
BTEMP	0		1.4	V	Battery temperature indication 100k pullup resistor to VREF in phone Battery package has NTC pull down resistor: 47kΩ °+/-5%@+25°C , B=4050+/-3%
	2.1 5	 10	3 20	V ms	Phone power up by battery (input) Power up pulse width
	1.9 90	 100	2.8 200	V ms	Battery power up by phone (output) Power up pulse width
	-5		5	%	100k pull-up resistor tolerance

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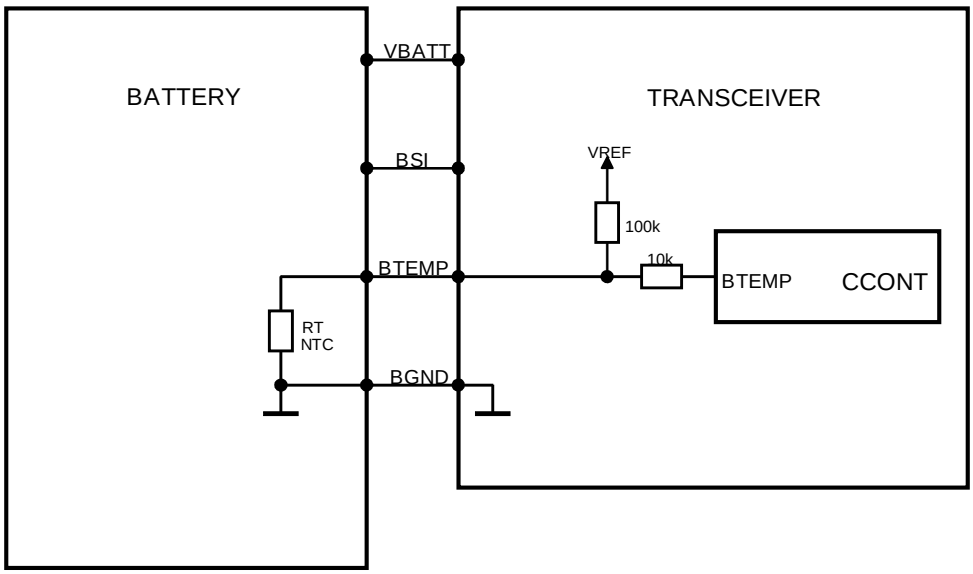

Figure 9: Standard battery - BTEMP connection

Based on 47kΩ ± 5 % NTC with B = 4050 ±3 %. ***Without any alignment***, with that and 1 % pull-up resistor, ± 2.5 °C accuracy is achieved between - 20 and +60 °C (± 3.5 °C @ -40 ... +85 °C).

Supply Voltage Regulators

The heart of the power distribution is the CCONT. It includes all the voltage regulators and feeds the power to the whole system. The baseband digital parts are powered from the VBB regulator which provides 2.8V baseband supply. The baseband regulator is active always when the phone is powered on. The VBB baseband regulator feeds MAD and memories, COBBA digital parts and the LCD driver in the UI section. There is a separate regulator for the SIM card. The regulator is selectable between 3V and 5V and controlled by the SIMPwr line from MAD to CCONT. The COBBA analog parts are powered from a dedicated 2.8V supply VCOBBA. The CCONT supplies also 5V for RF.
The CCONT contains a real time clock function.

Table 12: Regulator activity -different operating modes

Operating mode	Vref	RF REG	VCOBBA	VBB	VSIM	SIMIF
Power off	Off	Off	Off	Off	Off	Pull down
Power on	On	On/Off	On	On	On	On/Off
Reset	On	Off VR1 On	On	On	Off	Pull down
Sleep	On	Off	Off	On	On	On/Off

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CCONT includes also five additional 2.8V regulators providing power to the RF section. These regulators can be controlled either by the direct control signals from MAD or by the RF regulator control register in CCONT which MAD can update.
CCONT generates also a 1.5 V reference voltage VREF to COBBA. The VREF voltage is also used as a reference to some of the CCONT A/D converters.

Table 13: Regulators output voltage characteristics

Characteristics	Condition	Min	Typ	Max	Unit
Output current VR1-VR6	Vout@2.8V			80	mA
Output current VR7 Depends on external BJT	Vout@2.8V			150	mA
Output current VR7BASE Base current limit	Vout@2.8V			-10	mA
Output current VBB On Current limit 250mA Output current VBB Sleep Current limit 5mA	Vout@2.8V Vout@2.8V			125 1	mA mA
Output voltage VR1-VR7	over full temperature, input voltage and load range	2.7	2.8	2.85	V
Output voltage VBB	over full temperature, input voltage and load range	2.7	2.8	2.85	V
Line regulation (not VBB)	F v 10kHz, 2) VBAT>3.15V	49			dB
Line regulation (not VBB)	F v 100kHz, 2) VBAT>3.15v	40			dB
Line regulation VBB	F v 100kHz 2)	30			dB
Load regulation	T = 25°C		0.6	1	mV/mA
Supply current (each regulator) VR1...VR7	ON mode		I_{out}/ 60+330	I_{out}/ 10+540	mA
Supply current VBB	ON mode		I_{out}/60+ 250	I_{out}/10+ 400	mA
Supply current VBB	SLEEP mode		I_{out}/60+ 100	I_{out}/10+ 150	mA

Note 1: *Characteristics above are NOT valid if Vbat < 3.0V.*

Note 2: *Line regulation is 20dB for f<100kHz when battery voltage is lower than 3.1V.*

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Switched Mode Power Supply VSIM

There is a switched mode supply for SIM-interface. SIM voltage is selected via serial IO. The 5V SMR can be switched on independently of the SIM voltage selection, but can't be switched off when VSIM voltage value is set to 5V.

Table 14: Electrical characteristics - VSIM and V5V

Characteristics	Condition	Min	Typ	Max	Unit
Output voltage VSIM	Over temperature Over current	2.8 4.8	3.0 5.0	3.2 5.2	V
Output voltage V5V	Over temp & current	4.8	5.0	5.2	V
Output voltage V5V_2	Over temperature	5.0		6.0	V
Output current VSIM	Continuous DC			30	mA
Output current V5V	Continuous DC			30	mA
current consumption VSIM	on sleep		200 100	330 150	uA uA

Note: *VSIM and V5V can give together a total of 30mA.*

SMR / VSIM-functions is shown In the figure below .

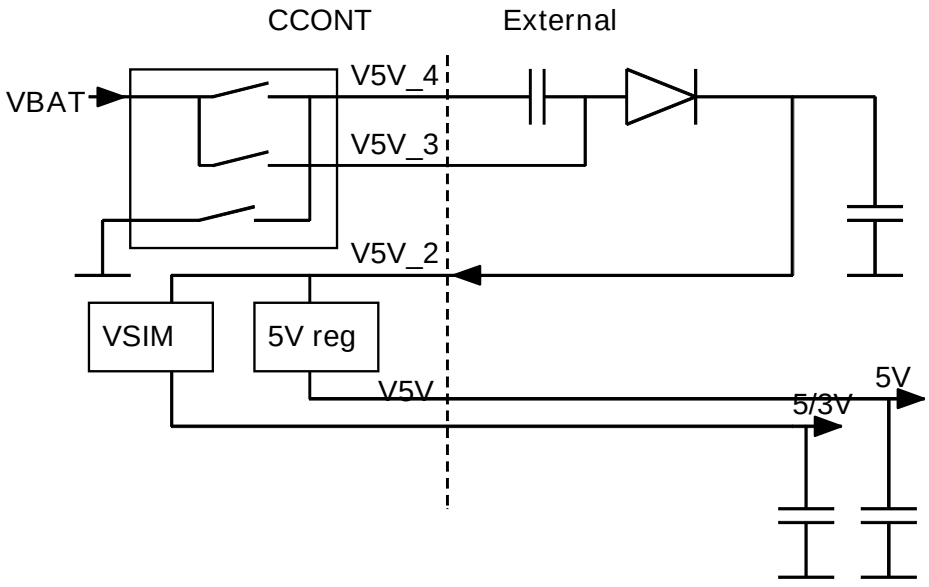

Figure 10: SMR power functions

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Power Up and Power Down

When the PURX reset is released, the MAD releases the system reset ExtSysResetX and the internal MCUResetX signals and starts the boot program execution.
The logic-level on the GenSDIO pin of the MAD select where the BOOT program execution starts :

GenSDIO = '0' : from MAD boot-ROM
GenSDIO = '1' : from external memory.

In normal operation the program execution continues from the flash program memory, but If the MBUS line is pulled low during the power up, then the boot-ROM starts a flash programming sequence and waits for the prommer response through FBUS_RX line.

The baseband is powered up by:

1. Pressing the power key, that generates a PWRONX signal from the power key to the CCONT, which starts the power up procedure.

2. Connecting a charger to the phone. The CCONT recognizes the charger from the VCHAR voltage and starts the power up procedure.

3. A RTC interrupt. If the real time clock is set to alarm and the phone is switched off, the RTC generates an interrupt signal, when the alarm is gone off. The RTC interrupt signal is connected to the PURX line to give a power on signal to the CCONT just like the power key.

4. A battery interrupt. Intelligent battery packs have a possibility to power up the phone. When the battery gives a short (10ms) voltage pulse through the BTEMP pin, the CCONT wakes up and starts the power on procedure.

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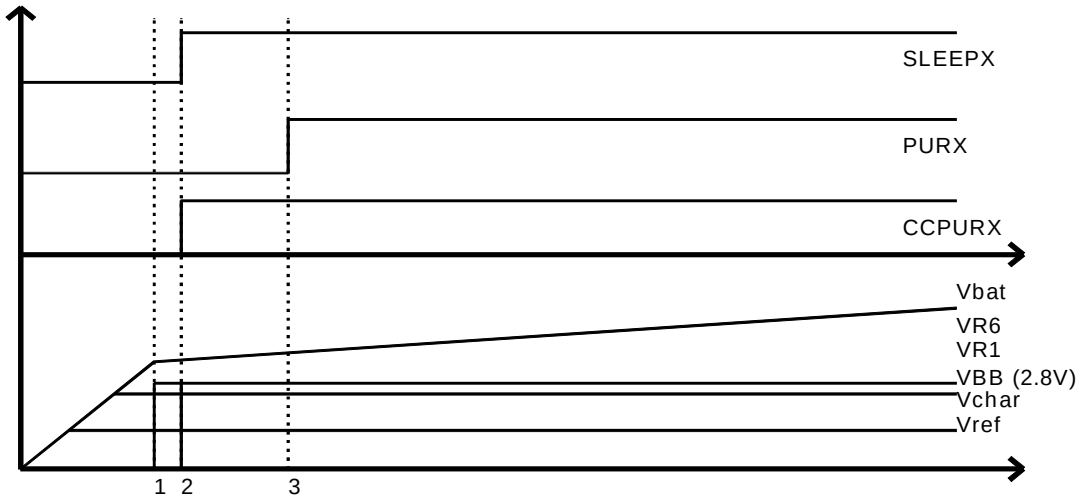
Power Up with a Charger

When the charger is connected, CCONT will switch on the CCONT digital voltage as soon as the battery voltage exceeds 3.0V. The reset for CCONT's digital parts is released when the operating voltage is stabilized (50 us from switching on the voltages). Operating voltage for VCXO is also switched on. The counter in CCONT digital section will keep MAD in reset for 62 ms (PURX) to make sure that the clock provided by VCXO is stable. After this delay MAD reset is released, and VCXO -control (SLEEPX) is given to MAD. The next diagram explains the power on procedure with charger (the picture assumes empty battery, but the situation would be the same with full battery):



1: Battery voltage over 3.0==>Digital voltages to CCONT
2: CCONT digital reset released. VCXO turned
3: 62ms delay before PURX

Figure 11: Power up with charger

When the phone is powered up with an empty battery pack using the standard charger, the charger may not supply enough current for standard power-up procedure and the power-up must be delayed.

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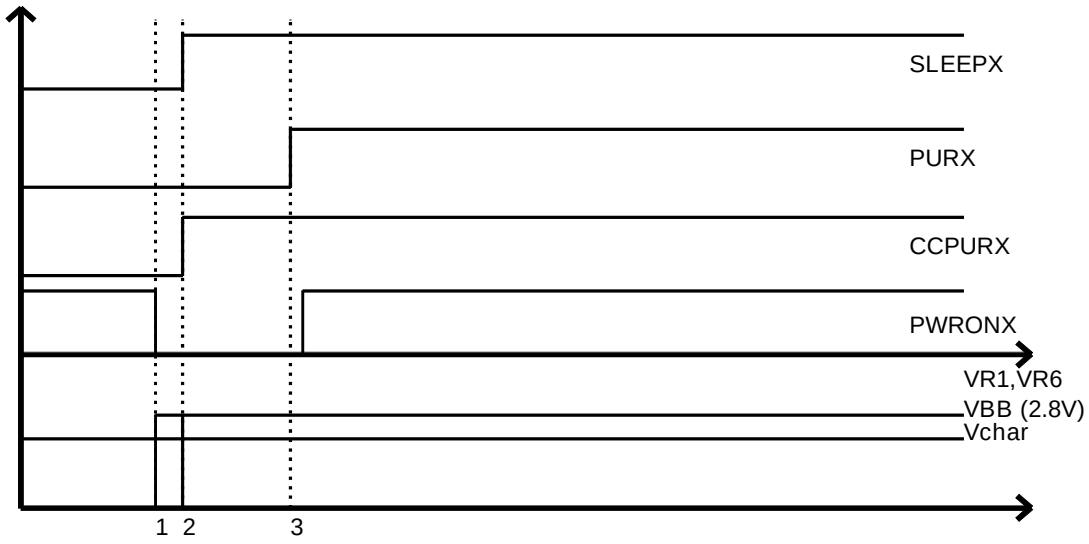
Power Up with Power Switch (PWRONX)

When the power on switch is pressed the PWRONX signal will go low. CCONT will switch on the CCONT digital section and VCXO as was the case with the charger driven power up. If PWRONX is low when the 62 ms delay expires, PURX is released and SLEEPX control goes to MAD. If PWRONX is not low when 62 ms expires, PURX will not be released, and CCONT will go to power off (digital section will send power off signal to analog parts)



1: Power switch pressed ==> Digital voltages on in CCONT.
2: CCONT digital reset released. VCXO turned on.
3: 62 ms delay.

Figure 12: Power up with switch

Power Up by IBI

IBI can power CCONT up by giving a short pulse (10ms) through the BTEMP line. After power-up BTEMP will act as any other input channel for ADC.

Power Down

The baseband is powered down by:

1 Pressing the power key, that is monitored by the MAD, which starts the power down procedure.

2 If the battery voltage is dropped below the operation limit, either by not charging it or by removing the battery.

3 Letting the CCONT watchdog expire, which switches off all CCONT regulators and the phone is powered down.

4 Setting the real time clock to power off the phone by a timer. The RTC generates an interrupt signal, when the alarm is gone off. The RTC interrupt signal is connected to the PWRONX line to give a power off signal to the CCONT just like the power key.

The power down is controlled by the MAD. When the power key has been pressed long enough or the battery voltage is dropped below the limit the MCU initiates a power down procedure and disconnects the SIM power. Then the MCU outputs a system reset signal and resets the DSP. If there is no charger connected the MCU writes a short delay to CCONT watchdog and resets itself. After the set delay the CCONT watchdog expires, which activates the PURX and all regulators are switched off and the phone is powered down by the CCONT.

Modes of Operation

Acting Dead

If the phone is off or switched off when the charger is connected, the phone is powered on but enters a state called "acting dead". To the user the phone acts as if it was switched off. A battery charging alert is given and/or a battery charging indication on the display is shown to acknowledge the user that the battery is being charged.

Active Mode

In the active mode the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. All the CCONT regulators are operating. There are several sub-states in the active mode depending on if the phone is in burst reception, burst transmission, if DSP is working etc.

Sleep Mode

In the sleep mode all the regulators except the baseband VBB and the SIM card VSIM regulators are off. Sleep mode is activated by the MAD after MCU and DSP clocks have been switched off. The voltage regulators for the RF section are switched off and the VCXO power control, VCXOPwr is set low. In this state only the 32 kHz sleep clock oscillator in CCONT is running. The flash memory power down input is connected to the ExtSysResetX signal, and the flash is deep powered down during the sleep mode.

The sleep mode is exited either by the expiration of a sleep clock counter in the MAD or by some external interrupt, generated by a charger connection, key press, headset connection etc. The MAD starts the wake up sequence and sets the VCXOPwr and ExtSysResetX control high. After VCXO settling time other regulators and clocks are enabled for active mode.

If the battery pack is disconnect during the sleep mode, the CCONT pulls the SIM interface lines low as there is no time to wake up the MCU.

Charging

Charging can be performed in any operating mode. The battery type/size is indicated by a resistor inside the battery pack. The resistor value corresponds to a specific battery capacity. This capacity value is related to the battery technology as different capacity values are achieved by using different battery technology.

The battery voltage, temperature, size and current are measured by the CCONT controlled by the charging software running in the MAD.

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The power management circuitry controls the charging current delivered from the charger to the battery. Charging is controlled with a PWM input signal, generated by the CCONT. The PWM pulse width is controlled by the MAD and sent to the CCONT through a serial data bus. The battery voltage rise is limited by turning the CHAPS switch off when the battery voltage has reached V. Charging current is monitored by measuring the voltage drop across a 220 Mohm resistor.

Watchdog

The Watchdog block inside CCONT contains a watchdog counter and some additional logic which are used for controlling the power on and power off procedures of CCONT. Watchdog output is disabled when WDDisX pin is tied low, - the WD–counter runs during that time, though.
Watchdog counter is reset internally to 32 sec. at power up. Normally it is reset by MAD writing a control word to the WDReg.

Audio Control

PCM Serial Interface

The interface consists of following signals:

- PCM codec master clock (PCMDClk),
- frame synchronization signal to DSP (PCMSClk),
- codec transmit data line (PCMTX)
- codec receive data line (PCMRX).

The COBBA-GJP generates the PCMDClk clock, which is supplied to DSP SIO. The COBBA-GJP also generates the PCMSClk signal to DSP by dividing the PCMDClk. The PCMDClk frequency is 1.000 MHz and is generated by dividing the RFIClk 13 MHz by 13. The COBBA-GJP further divides the PCMDClk by 125 to get a PCMSClk signal, 8.0 kHz.

Figure 13: Audio Control

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Digital Control

The baseband functions are controlled by the MAD ASIC, which consists of a MCU, a system ASIC and a DSP. MAD with the GSM/PCN specific ASIC is named to MAD2.

- MAD2 WD1
- MAD2 WD1 contains following building blocks:
- ARM RISC processor with both 16-bit instruction set (THUMB mode) and 32-bit instruction set (ARM mode)
- TI Lead DSP core with peripherals:
- API (Arm Port Interface memory) for MCU-DSP communication, DSP code download, MCU interrupt handling vectors (in DSP RAM) and DSP booting.
- Serial port (connection to PCM)
- Timer
- DSP memory
- BUSC (Bus Controller for controlling accesses from ARM to API, System Logic and MCU external memories, both 8- and 16-bit memories)
- System Logic
- CTSI (Clock, Timing, Sleep and Interrupt control)
- MCUIF (Interface to ARM via BUSC). Contains MCU Boot-ROM
- DSPIF (Interface to DSP)
- MFI (Interface to COBBA AD/DA Converters)
- CODER (Block encoding/decoding and A51&A52 ciphering)
- AccIF(Accessory Interface)
- SCU (Synthesizer Control Unit for controlling 2 separate synthesizer)
- UIF (Keyboard interface, serial control interface for COBBA PCM Codec, LCD Driver and CCONT)
- SIMI (SimCard interface with enhanced features)
- PUP (Parallel IO, USART and PWM control unit for vibra and buzzer)
- Flexpool

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The MAD2 operates from a 13 MHz system clock, which is generated from the 13Mhz VCXO frequency. The MAD2 supplies a 6,5 MHz or a 13 MHz internal clock for the MCU and system logic blocks and a 13 MHz clock for the DSP, where it is multiplied to 45.5 MHz DSP clock. The system clock can be stopped for a system sleep mode by disabling the VCXO supply power from the CCONT regulator output. The CCONT provides a 32 kHz sleep clock for internal use and to the MAD2, which is used for the sleep mode timing. The sleep clock is active when there is a battery voltage available i.e. always when the battery is connected.

Memories

MAD Memory Configuration

The MAD2WD1 used in Hda52 contains 16 kW RAM, and 80 kW ROM memory.

Memory

The MCU program code resides in an external flash program memory, which size is 16Mbits (1024k x 16bit). The MCU work (data) memory size is 1024 kbits (64 x 16bit). The Bus Controller (BUSC) section in the MAD decodes the chip select signals for the external memory devices and the system logic. BUSC controls internal and external bus drivers and multiplexers connected to the MCU data bus. The MCU address space is divided into access areas with separate chip select signals. BUSC supports a programmable number of wait states for each memory range.

Program and Data Memory

The MCU program code resides in the program memory. The program memory is 16Mbits (1024k x 16bit) Flash memory.

The flash memory has a power down pin that should be kept low, during the power up phase of the flash to ensure that the device is powered up in the correct state, read only. The power down pin is utilized in the system sleep mode by connecting the ExtSysResetX to the flash power down pin to minimize the flash power consumption during the sleep.

Nonvolatile data memory is implemented with program (Flash) memory. Special EEPROM emulation (EEEMmu) software is utilized.

Work Memory

The work memory is a static RAM of size 1024k (64k x 16). The memory contents are lost when the baseband voltage is switched off. All retainable data must be stored into the data memory when the phone is powered down.

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MCU Memory Requirements

Table 15: Memory Requirements

Device	Organization	Access Time ns	Wait States Used	Remarks
FLASH	1024kx16	120	1	UBGA 48
SRAM	64kx16	120	1	UBGA 48

MCU Memory Map

MAD2 supports maximum of 4GB internal and 4MB external address space. External memories use address lines MCUAd0 to MCUAd21 and 8-bit/16-bit databus. The BUSC bus controller supports 8- and 16-bit access for byte, double byte, word and double word data. Access wait states (0, 1 or 2) and used databus width can be selected separately for each memory block.

Flash Programming

The phone have to be connected to the flash loading adapter so that supply voltage for the phone and data transmission lines can be supplied from/to the adapter. When adapter switches supply voltage to the phone, the program execution starts from the BOOT-ROM and the MCU investigates in the early start-up sequence if the flash prommer is connected. This is done by checking the status of the MBUS-line. Normally this line is high but when the flash prommer is connected the line is forced low by the prommer.

The flash prommer serial data receive line is in receive mode waiting for an acknowledgement from the phone. The data transmit line from the baseband to the prommer is initially high. When the baseband has recognized the flash prommer, the TX-line is pulled low. This acknowledgement is used to start to toggle MBUS (FCLK) line three times in order that MAD2 gets initialized. This must be happened within 15 ms after TX line is pulled low. After that the data transfer of the first two bytes from the flash prommer to the baseband on the RX-line must be done within 1 ms.

When MAD2 has received the secondary boot byte count information, it forces TX line high. Now, the secondary boot code must be sent to the phone within 10 ms per 16 bit word. If these timeout values are exceeded, the MCU (MAD2) starts normal code execution from flash. After this, the timing between the phone and the flash prommer is handled with dummy bites.

Table 16: Flash programming timing characteristics

Characteristics	Min	Typ	Max	Unit
Time from boot indication to MAD2 initialization sequence			15	ms
Time from MAD2 initialization sequence to byte lenght information			1	ms
Time from byte length information to end of secondary boot code loading.			10 per16 bit word	ms

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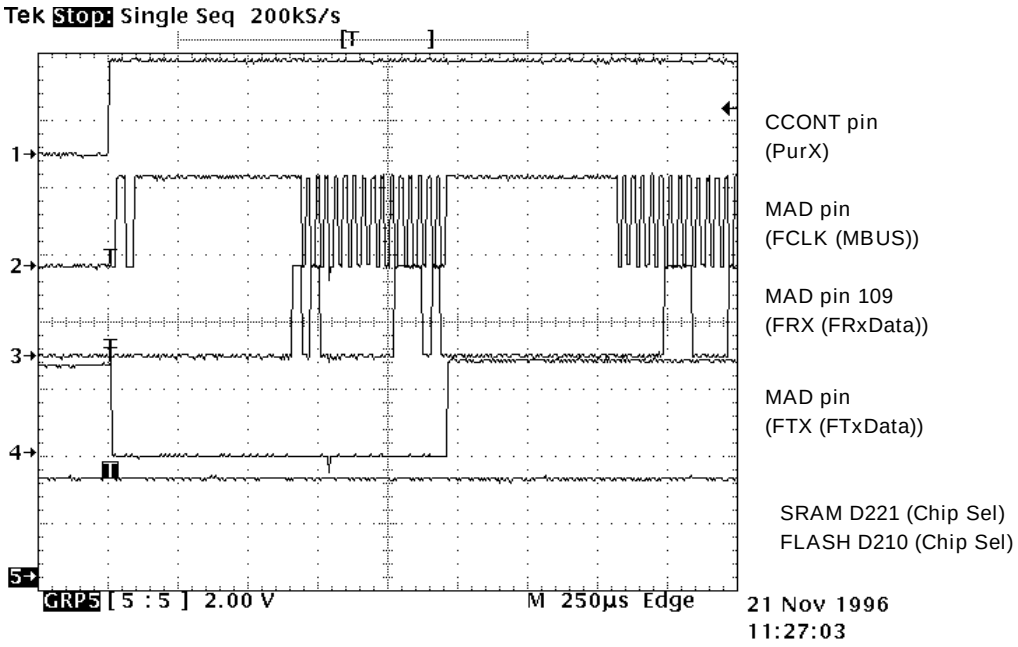

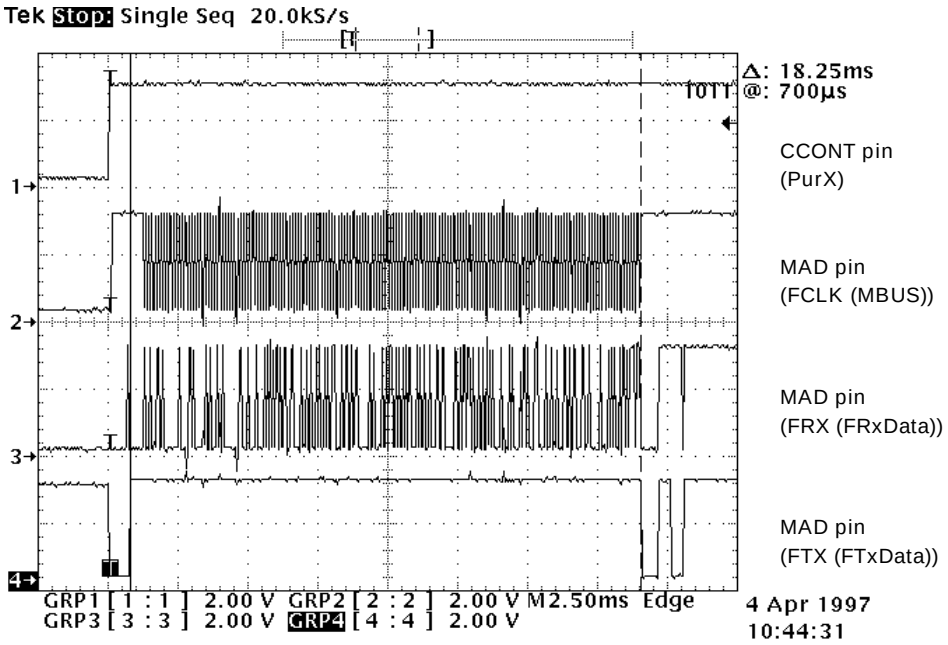
Tek Stop: Single Seq 20.0kS/s
Δ: 18.25ms
@: 700µs
CCONT pin
(PurX)
MAD pin
(FCLK (MBUS))
MAD pin
(FRX (FRxData))
MAD pin
(FTX (FTxData))
GRP1 [1 : 1] 2.00 V GRP2 [2 : 2] 2.00 V M2.50ms Edge
GRP3 [3 : 3] 2.00 V GRP4 [4 : 4] 2.00 V
4 Apr 1997
10:44:31

Figure 14: Flash programming sequence

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COBBA GJP

COBBA GJP ASIC provides an interface between the baseband and the RF-circuitry. COBBA performs analogue to digital conversion of the receive signal. For transmit path COBBA performs digital to analogue conversion of the transmit amplifier power control ramp and the in-phase and quadrature signals. A slow speed digital to analogue converter will provide automatic frequency control (AFC).

COBBA is at any time connected to MAD asic with two interfaces, one for transferring TX and RX data between MAD and COBBA and one for transferring codec RX/TX samples.

Real time clock

Requirements for a real time clock implementation are a basic clock (hours and minutes), a calendar and a timer with alarm and power on/off -function and miscellaneous calls. The RTC will contain only the time base and the alarm timer but all other functions (e.g. calendar) will be implemented with the MCU software.

The CCONT is an ideal place for an integrated real time clock as the asic already contains the power up/down functions and a sleep control with the 32kHz sleep clock, which is running always when the phone battery is connected. This sleep clock is used for a time source to a RTC block.

User Interface (UI)

The following circuits belongs to UI :

- LCD Module
- Keyboard
- Backlight circuit (for Keyboard and Display)
- Power key
- UI-Switch

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LCD Module

The display circuit includes LCD module GD47 (84x48 pixels) and two capacitors. The LCD module is COG (Chip on Glass) technology. The connection method for chip on the glass is ACF, Adhesive Conductive Film. The LCD module is connected to the PCB with spring contacts. Capacitors are placed on PCB.

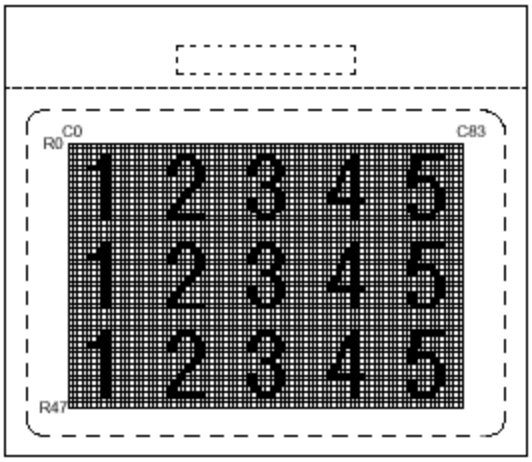

Figure 15: Display layout

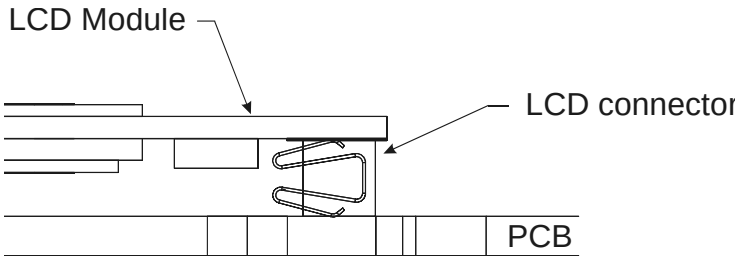

Figure 16: LCD connector

The display driver includes hw-reset, voltage tripler or quadrupler which depends on temperature, temperature compensating circuit and low power control. Driver includes 84x48 bit RAM memory which is used when some elements are created on display. Elements can be created with software. Driver doesn't include CG-ROM. One bit in RAM is same as one pixel on display.

Keyboard

Has 16 keys and uses 4 rows and 5 columns. Scanning is used for keyboard reading. Rows and columns are connected to MAD interface.

The 'Key-domes' which are connected to the ROW-signals from the MAD are sensible to ESD and are protected by a ESD network (ESDA6V1W5). Also serial resistors of 1K are inserted between the Keyboard Rows and the MAD.

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Table 17: HDa52 key matrix

	COL 0	COL 1	COL 2	COL 3	COL 4
ROW 0					
ROW 1	Up	Down			3
ROW 2	0		6	9	#
ROW 3		2	5	8	Soft-A
ROW 4	Clear	1	4	7	*
ROW 5					

Power Key

Power key is connected between GND and CCONT-pin 'PWRONX/ WDDISX'. Power switch is active in LOW state. Power key circuit is shown in Figure 15. Power key is connected to ROW1.

Backlight for Display and Keyboard

Display Backlight is made by four LEDs (in bottom of the Display).
Keyboard Backlight is made by 5 LEDs.

Color of all LEDs is yellow-green, λ = 570nm

Switching circuits for Display and keyboard back-light is controlled by the same signal: KBLIGHTS.
KBLIGHT-signal = HIGH -> the lights are on
KBLIGHT-signal = LOW -> the lights are off.
UISWITCH is used for controlling backlight.

Table 18: Display/keyboard backlight

Line Symbol	Parameter	Minimum	Typical / Nominal	Maximum	Unit	Notes
VB	Battery voltage	3.0		4.8	V	Same supply for Buzzer & Display
		50	55	60	mA	LEDs

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UI-Switch

Detailed description of the UISWITCH is given in document /16/.

The UISWITCH is an integrated switch IC for UI (user interface) purposes. It includes control switch for buzzer and vibra , LED-control (display & keyboard) and two current sinks for LED's.

Features :

- 2 adjustable constant current sink (60mA each) for keyboard and LCD-LEDs
- LED ON/OFF control (separated for keyboard and LCD)
- Buzzer ON/OFF control
- FET switch (low Rds-on) for buzzer current
- Vibra ON/OFFcontrol
- FET switch for vibra current
- Thermal shutdown
- Power down function for optimum current consumption
- Package TSSOP20 because of 1.5mm height requirement

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RF Module

NPB-1NB's direct conversion receiver and transmitter RF sections are described in this section. RF architecture contains an RF-IC ("Hagar"), a PA module, a VCO module, a VCTCXO module and a discrete LNA stage.

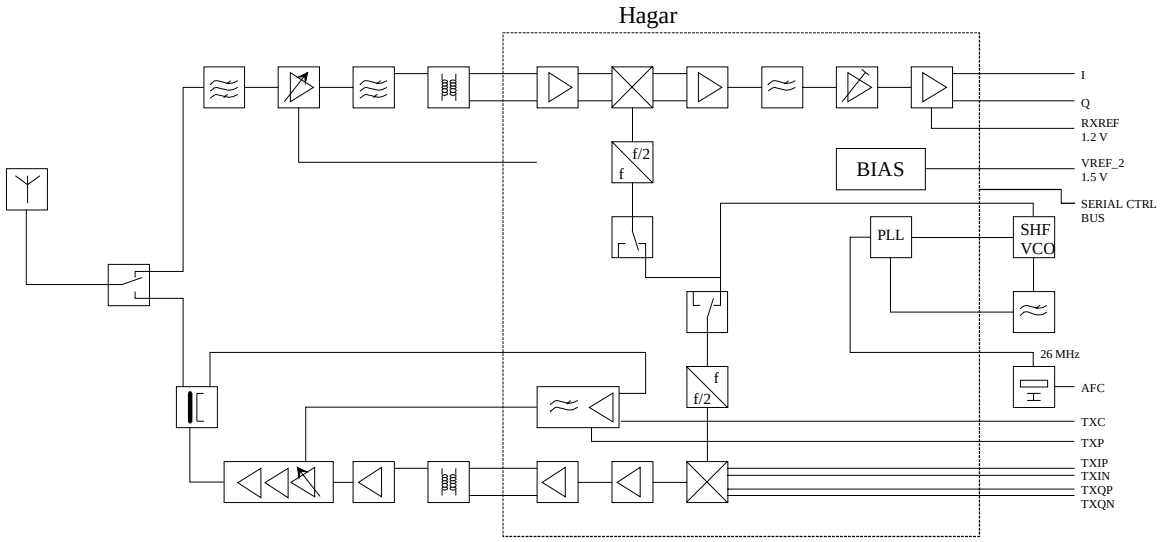

Figure 17: RF Block Diagram

Frequency Synthesizer

VCO frequency is locked by PLL into a stable frequency source which is a VCTCXO module (Voltage Controlled Temperature Compensated Crystal Oscillator). VCTCXO is running at 26 MHz. Temperature effect is controlled by AFC (Automatic Frequency Control) voltage. VCTCXO is locked to a frequency of base station. AFC is generated by baseband with an 11 bit conventional DAC in COBBA asic.

PLL is located in HAGAR RF-IC and is controlled via serial bus by COBBA (in baseband). There is a 64/65 (P/P+1) prescaler, an N- and A-divider, a reference divider, a phase detector and a charge pump for an external loop filter. SHF (Super High Frequency) local signal (twice the actual RF channel frequency), generated by a VCO module (Voltage Controlled Oscillator), is fed to the prescaler. The prescaler is a dual modulus divider. Output of the prescaler is fed to the N- and A-divider which generates an input to the phase detector. The phase detector compares this signal to a reference signal (400kHz) which is divided by the reference divider from VCTCXO output. Output of the phase detector is connected to the charge pump which charges or discharges an integrator capacitor in the loop filter depending on a phase of measured frequency compared to the reference frequency.

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Receiver

Receiver is a direct conversion linear receiver. Received RF signal from antenna is fed via a RF Antenna Switch to the 1st RX SAW filter and a discrete LNA (Low Noise Amplifier). Gain selection control of the LNA comes from HAGAR IC. Gain step is activated when RF level in antenna is about -43 dBm.

After the LNA amplified signal (with low noise level) is fed to a bandpass filter (the 2nd RX SAW filter). These bandpass filtered signals are then balanced with baluns. Differential RX signal is amplified and mixed directly down to a BB frequency in HAGAR. Local Oscillator signal is generated by an external VCO. The VCO signal is divided by 2. PLL and dividers are in HAGAR IC.

From the mixer output to an ADC input RX signal is divided to I- and Q-signals. Accurate phasing is generated by LO dividers. After the mixer DTOS amplifiers convert the differential signals to single ended. DTOS has two gain stages. The first one has constant gain of 12dB and 85kHz cut off frequency. The gain of second stage is controlled by control signal g10. If g10 is high (1) the gain is 6dB and if g10 is low (0) the gain is -4dB.

The active channel filters in HAGAR IC provides selectivity for channels (-3dB @ +/-100 kHz typ.). Integrated baseband filter is an active RC filter with two off-chip capacitors. Long RC time constant needed in the channel selection filter of direct conversion receiver is produced by large off-chip capacitors because the impedance levels could not be increased due to noise specifications.

The baseband filter consists of two stages, DTOS and BIQUAD. DTOS is a differential to single-ended converter having 8dB or 18dB gain. BIQUAD is a modified Sallen-Key Biquad.

Integrated resistors and capacitors are tunable. These are controlled by a digital control word. The correct control words which compensate process variation of the integrated resistors and capacitors and tolerance of the off-chip capacitors are found by a calibration circuit.

The next stage in receiver chain is an AGC amplifier - also integrated in HAGAR. The AGC has a digital gain control via serial bus from COBBA IC. The AGC stage provides gain control range of 40 dB (10 dB steps) for the receiver and also necessary DC compensation. The 10 dB AGC step is implemented by DTOS stages.

The DC compensation is made during DCN1 and DCN2 operations (controlled via serial bus). DCN1 is carried out by charging large external capacitors in the AGC stages to a voltage which cause a zero dc-offset. DCN2 sets the signal offset to a constant value (RXREF 1.2 V). The RXREF signal (from COBBA GJP) is used as a zero level to RX ADCs.

Single ended filtered I/Q-signal is finally fed to the ADCs of COBBA. The input level for ADC is 1.4 Vpp max.

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Transmitter

Transmitter chain consists of a final frequency IQ-modulator, a single band power amplifier and a power control loop.

I- and Q-signals are generated by baseband in COBBA asic. After post filtering (RC network) the signals are modulated by IQ-modulator in HAGAR IC. The LO signal for modulator is generated by a VCO and is divided by 2. After modulator the TX signal is amplified and buffered. HAGAR TX output level is +3 dBm minimum.

Next the TX signal is converted to single ended by discrete baluns. Following this, the power amplifier (PA) performs final amplification. It has a 50 ohm input and output. Proper output power is controlled by a power control loop. The PA is able to generate over 1 W output power (0 dBm input level). The gain control range is over 35 dB to get desired power levels and power ramping up/down.

Harmonics generated by the nonlinear PA are filtered out by the diplexer inside the antenna switch module. Power control circuitry consists of a discrete power detector and an error amplifier (in HAGAR). There is a directional coupler between the PA output and the antenna switch. The directional coupler takes a sample from the TX power with a certain ratio. The sampled signal is rectified by a schottky-diode to produce a DC signal (after filtering). The detected voltage is compared by the error amplifier in HAGAR to TXC voltage which is generated by a DA converter in COBBA. The TXC has a raised cosine form (cos4 function) which reduces switching transients when pulsing the TX power up and down.

Because dynamic range of the detector is not wide enough to control the TX power (actually the RF output voltage) over the whole range, there is a control named TXP to work under the detected levels. Burst is enabled and set to rise with TXP until the output level is high enough, i.e. when the feedback loop works. The loop controls the TX output to rise to a wanted output level. The burst has a template of the TXC ramp. Because the feedback loops can be unstable, the loop is compensated by a dominating pole. The pole decreases gain at high frequencies to insure phase margins are high enough.

AGC Strategy

AGC amplifier is used to maintain output level of the receiver in certain range. AGC has to be set before each received burst. This is called pre-monitoring. Receiver is switched on roughly 280 us before the burst begins. DSP measures received signal level and adjusts AGC amplifier via serial bus from COBBA GJP.

There is a 50 dB accurate gain control (10 dB steps) and one larger step (~30 dB) in LNA. LNA AGC gain step size depends on a channel with some amount.

RSSI must be measured accurately on range of -48...-110 dBm. Above -48 dBm level MS reports to base station the same reading.

Production calibration is done by two RF levels. The LNA gain step is not calibrated.

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AFC Function

AFC is used to lock the transceiver's clock to the frequency of the base station. AFC voltage is generated by COBBA asic with an 11 bit DA converter. In the AFC control line a RC filter is used to reduce noise coming from the converter. Settling time requirement for the RC network comes from signaling, i.e. how often PSW (Pure Sine Wave) slots occur. The PSW is repeated in every 10th frame. It means there is a PSW every 46 ms. The AFC tracks base station frequency continuously. This way the transceiver gets a stable frequency. Temperature does not quickly affect the VCTCXO frequency.

Settling time requirement comes also from the start-up time allowed. When the transceiver is in sleep mode and "wakes up" to a receive mode, there is only about 5 ms for the AFC voltage to settle. When the first burst comes in, the system clock has to be settled with +/- 0.1 ppm frequency accuracy. The VCTCXO module requires also 5 ms to settle to the final frequency. Amplitude rises to full swing in 1 ... 2 ms. Because the frequency settling time is higher, this oscillator must be powered up sufficiently early.

DC Compensation

DC compensation is done during DCN1 and DCN2 operations (controlled via serial bus). DCN1 operation is carried out by charging large external capacitors in the AGC stages to a voltage to reduce the dc offset. DCN2 sets the signal offset to a constant value (RXREF 1.2 V).

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Parts Lists

GB9_12 (PN. 0201513)
EDMS 3.10

Item	Code No.	Description	Value	Type
R100	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R101	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R102	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R103	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R104	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R105	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R106	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R107	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R108	1430746	Chip resistor	560	5 % 0.063 W 0402
R109	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R110	1620025	Res network 0w06 2x100k j		0404
R111	1620031	Res network 0w06 2x1k0 j		0404
R112	1430744	Chip resistor	470	5 % 0.063 W 0402
R113	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R114	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R116	1430734	Chip resistor	220	5 % 0.063 W 0402
R117	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R120	1430167	Chip resistor	47	5 % 0.063 W 0603
R121	1430167	Chip resistor	47	5 % 0.063 W 0603
R122	1430726	Chip resistor	100	5 % 0.063 W 0402
R130	1430710	Chip resistor	22	5 % 0.063 W 0402
R131	1430710	Chip resistor	22	5 % 0.063 W 0402
R155	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R200	1430728	Chip resistor	120	5 % 0.063 W 0402
R203	1430816	Chip resistor	330 k	5 % 0.063 W 0402
R204	1419003	Chip resistor	22	5 % 0.063 W 0402
R209	1430796	Chip resistor	47 k	5 % 0.063 W 0402

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Item	Code No.	Description	Value	Type
R210	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R211	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R212	1430826	Chip resistor	680 k	5 % 0.063 W 0402
R213	1620017	Res network 0w06 2x100r j		0404
R214	1430325	Chip resistor	2.2 M	5 % 0.063 W 0603
R217	1620017	Res network 0w06 2x100r j		0404
R220	1620019	Res network 0w06 2x10k j		0404
R221	1430808	Chip resistor	150 k	5 % 0.063 W 0402
R224	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R229	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R283	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R301	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R302	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R303	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R304	1620023	Res network 0w06 2x47k j		0404
R306	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R307	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R308	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R309	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R311	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R350	1430690	Chip jumper		0402
R401	1430389	Chip resistor	18	5 % 0.1 W 0603
R402	1430389	Chip resistor	18	5 % 0.1 W 0603
R403	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R404	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R405	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R406	1430726	Chip resistor	100	5 % 0.063 W 0402
R407	1430726	Chip resistor	100	5 % 0.063 W 0402
R414	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R415	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402

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Item	Code No.	Description	Value	Type
R416	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R417	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R450	1430389	Chip resistor	18	5 % 0.1 W 0603
R451	1430389	Chip resistor	18	5 % 0.1 W 0603
R500	1620003	Res network 0w03 4x100r j		0804
R501	1430728	Chip resistor	120	5 % 0.063 W 0402
R502	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R503	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R504	1620019	Res network 0w06 2x10k j		0404
R507	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R509	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R511	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R512	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R515	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R516	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R517	1430790	Chip resistor	27 k	5 % 0.063 W 0402
R518	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R519	1430718	Chip resistor	47	5 % 0.063 W 0402
R520	1430738	Chip resistor	270	5 % 0.063 W 0402
R521	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R522	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R525	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R526	1430738	Chip resistor	270	5 % 0.063 W 0402
R527	1620505	Res network 0w04		2DB ATT 0400404
R529	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R531	1430710	Chip resistor	22	5 % 0.063 W 0402
R535	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R536	1430730	Chip resistor	150	5 % 0.063 W 0402
R539	1430742	Chip resistor	390	5 % 0.063 W 0402
R540	1430730	Chip resistor	150	5 % 0.063 W 0402
R541	1620033	Res network 0w06 2x5k6 j		0404

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Item	Code No.	Description	Value	Type
R544	1430746	Chip resistor	560	5 % 0.063 W 0402
R548	1620033	Res network 0w06 2x5k6 j		0404
R553	1430720	Chip resistor	56	5 % 0.063 W 0402
R556	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R557	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R559	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R590	1430702	Chip resistor	12	5 % 0.063 W 0402
R591	1430742	Chip resistor	390	5 % 0.063 W 0402
R592	1430730	Chip resistor	150	5 % 0.063 W 0402
R601	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R604	1430690	Chip jumper		0402
R605	1430728	Chip resistor	120	5 % 0.063 W 0402
R606	1430690	Chip jumper		0402
R608	1430690	Chip jumper		0402
R743	1430690	Chip jumper		0402
C100	2320783	Ceramic cap.	33 n	10 % 10 V 0402
C101	2610207	Tantalum cap.	10 u	20 % 2.0x1.3x1.2
C102	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C103	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C104	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C105	2320783	Ceramic cap.	33 n	10 % 10 V 0402
C106	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C107	2610207	Tantalum cap.	10 u	20 % 2.0x1.3x1.2
C108	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C109	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C110	2320783	Ceramic cap.	33 n	10 % 10 V 0402
C111	2320783	Ceramic cap.	33 n	10 % 10 V 0402
C112	2610207	Tantalum cap.	10 u	20 % 2.0x1.3x1.2
C113	2320469	Ceramic cap.	1 u	Y5 V 0603
C114	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C115	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C116	2320805	Ceramic cap.	100 n	10 % 10 V 0402

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Item	Code No.	Description	Value	Type
C117	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C118	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C119	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C122	2315259	Chip array x5r 2x33n k 10v 0405		0405
C124	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C125	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C126	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C127	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C128	2610207	Tantalum cap.	10 u	20 % 2.0x1.3x1.2
C200	2611747	Tantalum cap.	10 u	20 % 10 V 2.0x1.3x1.5
C201	2611747	Tantalum cap.	10 u	20 % 10 V 2.0x1.3x1.5
C202	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C203	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C205	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C206	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C207	2320481	Ceramic cap.	5R 1 u	10 % 0603
C208	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C209	2320481	Ceramic cap.	5R 1 u	10 % 0603
C210	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C211	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C212	2320783	Ceramic cap.	33 n	10 % 10 V 0402
C213	2320481	Ceramic cap.	5R 1 u	10 % 0603
C214	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C215	2312411	Ceramic cap.	1.0 u	20 % 25 V 1206
C216	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C217	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C218	2310793	Ceramic cap.	2.2 u	10 % 10 V 0805
C219	2611747	Tantalum cap.	10 u	20 % 10 V 2.0x1.3x1.5
C220	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C221	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C222	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C223	2320546	Ceramic cap.	27 p	5 % 50 V 0402

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Item	Code No.	Description	Value	Type
C224	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C225	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C226	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C227	2611747	Tantalum cap.	10 u	20 % 10 V 2.0x1.3x1.5
C228	2611747	Tantalum cap.	10 u	20 % 10 V 2.0x1.3x1.5
C229	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C230	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C232	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C233	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C234	2320469	Ceramic cap.	1 u	Y5 V 0603
C235	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C236	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C237	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C238	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C239	2320481	Ceramic cap.	5R 1 u	10 % 0603
C240	2320481	Ceramic cap.	5R 1 u	10 % 0603
C241	2320481	Ceramic cap.	5R 1 u	10 % 0603
C242	2320481	Ceramic cap.	5R 1 u	10 % 0603
C243	2320481	Ceramic cap.	5R 1 u	10 % 0603
C244	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C245	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C246	2320481	Ceramic cap.	5R 1 u	10 % 0603
C290	2611755	Tantalum cap.	68 u	20 % 16 V 6.0x3.2x2.6
C303	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C304	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C305	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C306	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C307	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C308	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C309	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C310	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C311	2320805	Ceramic cap.	100 n	10 % 10 V 0402

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Item	Code No.	Description	Value	Type
C312	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C313	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C314	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C315	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C316	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C317	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C318	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C319	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C320	2320481	Ceramic cap.	5R 1 u	10 % 0603
C321	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C400	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C401	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C402	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C403	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C404	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C407	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C409	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C410	2309570	Ceramic cap.	1 u	Y5 V 1206
C411	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C413	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C414	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C415	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C416	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C417	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C418	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C421	2315201	Chip array np0 2x27p k 25v 0405		0405
C500	2611741	Tantalum cap.	4.7 u	20 % 10 V 2.0x1.3x1.2
C502	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C503	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C504	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C505	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C506	2320620	Ceramic cap.	10 n	5 % 16 V 0402

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Item	Code No.	Description	Value	Type
C507	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C508	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C509	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C510	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C511	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C512	2315019	Chip array np0 4x470p k 16v 0612		0612
C514	2315261	Chip array x5r 2x47n k 10v 0405		0405
C515	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C516	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C517	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C525	2320570	Ceramic cap.	270 p	5 % 50 V 0402
C526	2315251	Chip array x5r 2x180p k 16v 0405		0405
C529	2320783	Ceramic cap.	33 n	10 % 10 V 0402
C532	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C535	2320783	Ceramic cap.	33 n	10 % 10 V 0402
C536	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C540	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C542	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C543	2310793	Ceramic cap.	2.2 u	10 % 10 V 0805
C544	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C546	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C547	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C549	2610203	Tantalum cap.	2.2 u	20 % 10 V 2.0x1.3x1.2
C551	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C552	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C553	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C554	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C557	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C558	2312221	Ceramic cap.	4.7 n	5 % 25 V 0805
C559	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C560	2320552	Ceramic cap.	47 p	5 % 50 V 0402

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Item	Code No.	Description	Value	Type
C561	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C568	2320621	Ceramic cap.	0.5 p	0.25 % 50 V 0402
C569	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C570	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C571	2611741	Tantalum cap.	4.7 u	20 % 10 V 2.0x1.3x1.2
C572	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C573	2320596	Ceramic cap.	3.3 n	5 % 50 V 0402
C574	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C575	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C576	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C577	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C578	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C581	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C582	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C589	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C592	2312215	Ceramic cap.	2.2 n	5 % 50 V 0805
C601	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C602	2320805	Ceramic cap.	100 n	10 % 10 V 0402
C603	2320481	Ceramic cap.	5R 1 u	10 % 0603
C604	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C610	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C611	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C613	2320514	Ceramic cap.	1.2 p	0.25 % 50 V 0402
C615	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C692	2312211	Ceramic cap.	3.3 u	10 % 0805
C693	2312211	Ceramic cap.	3.3 u	10 % 0805
C712	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C713	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C717	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C752	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C759	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C765	2320540	Ceramic cap.	15 p	5 % 50 V 0402

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Item	Code No.	Description	Value	Type
C802	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C867	2320536	Ceramic cap.	10 p	5 % 50 V 0402
L201	3203701	Ferrite bead 33r/100mhz		0805
L202	3203701	Ferrite bead 33r/100mhz		0805
L400	3203709	Ferrite bead 0.5r 120r/ 100m		0402
L401	3203709	Ferrite bead 0.5r 120r/ 100m		0402
L404	3203801	Chip bead array 2x1000r		0405
L500	3646065	Chip coil	12.Q n	5 % Q=31/800 MHz 0402
L502	3646409	Chip coil	1.-0 n	Q=34/800M 0402
L506	3646041	Chip coil	2.-0 n	Q=8/100M 0402
L511	3648808	Chip coil	10.Q u	10 % Q=50 1206
L512	3646039	Chip coil	5.-0 n	Q=7/100M 0402
L513	3203705	Ferrite bead 0.015r 42r/ 100m		0805
L515	4551019	Dir.coup. 1880+-30mhz 1		4DB 2X1.22x1.25
L601	3646013	Chip coil	6. Q n	5 % Q=7/100 MHz 0402
L605	3646041	Chip coil	2.-0 n	Q=8/100M 0402
L606	3646015	Chip coil	8. Q n	5 % Q=7/100 MHz 0402
L752	3640043	Chip coil	4. Q n	10 % Q=50/1GHZ 0805
L758	3646027	Chip coil	33.Q n	5 % Q=7/100 MHz 0402
B200	4510219	Crystal	32.768 k	+-30PPM 9PF
G502	4510261	VCTCXO	26 M	+-5PPM 2.7V GSM
G503	4350237	Vco 3700-3980mhz 2.7v 20ma pcs		
F200	5119019	SM, fuse f 1.5a 32v		
Z500	4511167	Saw filter	1960+-30 M	
Z501	4511167	Saw filter	1960+-30 M	
Z502	4550203	Ant.switch 1850-1990mhz		
T500	3640431	Transf balun 1920mhz+/-70mhz		
T502	3640423	Transf balun 3.7ghz+/-300mhz		0805

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Item	Code No.	Description	Value	Type
T503	3640431	Transf balun 1920mhz+/-70mhz		0805
V100	4210100	Transistor	BC848W	npn 30 V SOT323
V101	4210119	Transistor	BC849CW	npn 30 V 0.1 A SOT323
V102	4210052	Transistor	DTC114EE	npn RB V EM3
V201	1825023	Chip varistor vwm9v vc20v 0805		0805
V202	4110067	Schottky diode	MBR0520L	20 V 0.5 A SOD123
V203	4113671	Tvs esda6v1w5		**
V204	4113671	Tvs esda6v1w5		**
V402	4110089	Diode x 2	BAV70W	70 V .5 A 4 ns SOT323
V403	4864471	Led	Green	1305
V404	4864471	Led	Green	1305
V407	4864471	Led	Green	1305
V408	4864471	Led	Green	1305
V409	4864471	Led	Green	1305
V410	4864471	Led	Green	1305
V411	4864471	Led	Green	1305
V412	4864471	Led	Green	1305
V414	4110601	Diode	FAST	SOD323
V415	4113671	Tvs esda6v1w5		**
V416	4113671	Tvs esda6v1w5		**
V500	4210119	Transistor	BC849CW	npn 30 V 0.1 A SOT323
V501	4210185	Transistor		SOT343
V502	4210119	Transistor	BC849CW	npn 30 V 0.1 A SOT323
V503	4110078	Schdix2 bas70-05w 70v 70ma		SOT323
V504	4219929	Transistor x 2	2+4X10K	npn UM V SOT363
D300	4370677	Mad2wd1 v18 rom5 f741541g		UBGA144
D301	4340585	IC, flash mem.		UBGA48
D302	4340903	IC, SRAM		CSP48
D303	4340413	IC, regulator	TK11230BMC	3.0 V SOT23L
D304	4340761	IC, MCU	MC33464N	SOT23-5

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Item	Code No.	Description	Value	Type
N100	4370643	Cobba_gjp v4.1 v257bg64t/8 bga64		BGA64
N200	4370621	Chaps v2.0 u423v20g36t lbga6x6		
N201	4370719	Ccont 2m wfd163mg64t/ 8 lfbga8x8		
N400	4370433	Uiswitch sttm23av20t tssop20		TSSOP20
N500	4370731	Hagar 4 sttza8ig80t		LFBGA80
N502	4350241	IC, pow.amp.		
N503	4340719	IC, regulator	TK11247BMC	4.7 V SOT23L
S419	5209001	SM, sw tact spst 12v 50ma side k		KEY
X001	9510670	Pa shield assy		
X002	9510671	RF shield assy		
X003	9517063	Bb shield assy		
	9854477	PCB GB9		

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